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EXAMINER	
SHEW, JOHN	
ART UNIT	**PAPER NUMBER**
2664	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/820,351	SHINOHARA, MASAYUKI	
	Examiner	Art Unit	
	John L Shew	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/29/2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,8,10,12-18,20,21,23,25,26,29-34,36,37,39,41-47,49,50,52 and 54* is/are rejected.

7)☒ Claim(s) *6,9,11,19,22,24,27,28,35,38,40,48,51,53 and 55-58* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05182001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Page 21 line 2 cites "steps S4 to S6" should be "steps S14 to S16".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4, 5, 7, 14, 17, 18, 20, 30, 33, 34, 36, 43, 46, 47, 49 are rejected under 35 U.S.C. 102(b) as being anticipated by Kerr et al. (Patent number 6513108).

Claim 1, Kerr teaches a method of carrying out arbitration in a packet exchanger (FIG. 2, column 6 lines 22-37, column 7 lines 31-42) referenced by the arbiter 255 of the network switch which is a packet exchanger, including an input buffer temporarily storing a packet having arrived at an input port (FIG. 2, FIG. 3, column 8 lines 36-60)

referenced by the Input Header Buffer 700 receiving input data via the Buffer and Queuing Unit 210 from the input ports, and a packet switch which switches a packet between a specific input port and a specific output port (FIG. 1, FIG. 2, column 5 lines 42-44) referenced by the router/switch 200, said method comprising the steps of (a) concurrently carrying out a first plurality of sequences in each of said sequences basic processes (FIG. 3, column 5 lines 45-49, column 8 lines 36-54, column 9 lines 53-56) referenced by the column of Processing Elements 400 operating in parallel of substantially the same function, for at least one of said input buffer (FIG. 3) referenced by the Input Header Buffer 700, and said output port, (FIG. 3) referenced by the Output Header Buffer 900, are carried out in a predetermined order (FIG. 3) referenced by the fixed row of PE 400 which determines the fixed order of processing, and (b) making an allowance in each of said sequences for packets to be output through output ports at different times from one another (FIG. 6, column 11 lines 3-22) referenced by the phase difference between rows for different output times to the Output Header Buffer 900.

Claim 4, Kerr teaches wherein said basic process is completed in a unit period of time defined as a period of time necessary for said input buffers to output a packet (FIG. 3, FIG. 6, column 11 lines 3-22) referenced by the time period of 6 columns for processing to the Output Header Buffer 900 to output from the switch, said basic process being carried out for at least one of said input buffers and said output ports in each of said sequences in said unit period of time (FIG. 3) referenced by the row for the Input

Header Buffers 700 to the Output Header Buffers for the unit of time of 6 processing elements.

Claim 5, Kerr teaches the step of concurrently carrying out a second plurality of sequences after said first plurality of sequences have been carried out (FIG. 3) referenced by the second column of Processing Elements 400 which are processed concurrently after the completion of the first column of Processing Elements.

Claim 7, Kerr teaches wherein said first plurality of sequences starts being carried out at a first time (FIG. 5) referenced by the Row 0 IHB to PE_0 starting at time t_1, and said second plurality of sequences starts being carried out at a second time later than said first time (FIG. 5, FIG. 6, column 11 lines 3-22) referenced by the shaded area after Row 5 which is the time for the second column PE processing corresponding to time t_9, by a predetermined period of time (column 11 lines 40-45) referenced by the completion of the first column PE processing with guard time of t_1-t_0.

Claim 14, Kerr teaches an arbiter circuit constituting a packet exchanger (FIG. 2, column 6 lines 22-37, column 7 lines 31-42) referenced by the arbiter 255 of the network switch which is a packet exchanger, together with an input buffer temporarily storing a packet having arrived at an input port (FIG. 2, FIG. 3, column 8 lines 36-60) referenced by the Input Header Buffer 700 receiving input data via the Buffer and Queuing Unit 210 from the input ports, and a packet switch which switches a packet

between a specific input port and a specific output port (FIG. 1, FIG. 2, column 5 lines 42-44) referenced by the router/switch 200, said arbiter circuit having functions of (a) concurrently carrying out a first plurality of sequences in each of said sequences basic processes (FIG. 3, column 5 lines 45-49, column 8 lines 36-54, column 9 lines 53-56) referenced by the column of Processing Elements 400 operating in parallel of substantially the same function, for at least one of said input buffer (FIG. 3) referenced by the Input Header Buffer 700, and said output port, (FIG. 3) referenced by the Output Header Buffer 900, are carried out in a predetermined order (FIG. 3) referenced by the fixed row of PE 400 which determines the fixed order of processing, and (b) making an allowance in each of said sequences for packets to be output through output ports at different times from one another (FIG. 6, column 11 lines 3-22) referenced by the phase difference between rows for different output times to the Output Header Buffer 900.

Claim 17, Kerr teaches an arbiter circuit wherein said basic process is completed in a unit period of time defined as a period of time necessary for said input buffers to output a packet (FIG. 3, FIG. 6, column 11 lines 3-22) referenced by the time period of 6 columns for processing to the Output Header Buffer 900 to output from the switch, said basic process being carried out for at least one of said input buffers and said output ports in each of said sequences in said unit period of time (FIG. 3) referenced by the row for the Input Header Buffers 700 to the Output Header Buffers for the unit of time of 6 processing elements.

Claim 18, Kerr teaches an arbiter circuit wherein the arbiter circuit includes a function of concurrently carrying out a second plurality of sequences after said first plurality of sequences have been carried out (FIG. 3) referenced by the second column of Processing Elements 400 which are processed concurrently after the completion of the first column of Processing Elements.

Claim 20, Kerr teaches an arbiter circuit wherein said arbiter circuit starts carrying out said first plurality of sequences at a first time (FIG. 5) referenced by the Row 0 IHB to PE_0 starting at time t_1, and said second plurality of sequences at a second time later than said first time (FIG. 5, FIG. 6, column 11 lines 3-22) referenced by the shaded area after Row 5 which is the time for the second column PE processing corresponding to time t_9, by a predetermined period of time (column 11 lines 40-45) referenced by the completion of the first column PE processing with guard time of t_1-t_0.

Claim 30, Kerr teaches a recording medium readable by a computer storing a program therein (FIG. 4) referenced by the Instruction Memory 420 readable by the Memory Manager computer in communication with the CPU Core 410, for causing a computer to carry out a method of carrying out arbitration in a packet exchanger (FIG. 2, column 6 lines 22-37, column 7 lines 31-42) referenced by the arbiter 255 of the network switch which is a packet exchanger, including an input buffer temporarily storing a packet having arrived at an input port (FIG. 2, FIG. 3, column 8 lines 36-60) referenced by the Input Header Buffer 700 receiving input data via the Buffer and Queuing Unit 210 from

the input ports, and a packet switch which switches a packet between a specific input port and a specific output port (FIG. 1, FIG. 2, column 5 lines 42-44) referenced by the router/switch 200, said method comprising the steps of (a) concurrently carrying out a first plurality of sequences in each of said sequences basic processes (FIG. 3, column 5 lines 45-49, column 8 lines 36-54, column 9 lines 53-56) referenced by the column of Processing Elements 400 operating in parallel of substantially the same function, for at least one of said input buffer (FIG. 3) referenced by the Input Header Buffer 700, and said output port, (FIG. 3) referenced by the Output Header Buffer 900, are carried out in a predetermined order (FIG. 3) referenced by the fixed row of PE 400 which determines the fixed order of processing, and (b) making an allowance in each of said sequences for packets to be output through output ports at different times from one another (FIG. 6, column 11 lines 3-22) referenced by the phase difference between rows for different output times to the Output Header Buffer 900.

Claim 33, Kerr teaches wherein said basic process is completed in a unit period of time defined as a period of time necessary for said input buffers to output a packet (FIG. 3, FIG. 6, column 11 lines 3-22) referenced by the time period of 6 columns for processing to the Output Header Buffer 900 to output from the switch, said basic process being carried out for at least one of said input buffers and said output ports in each of said sequences in said unit period of time (FIG. 3) referenced by the row for the Input Header Buffers 700 to the Output Header Buffers for the unit of time of 6 processing elements.

Claim 34, Kerr teaches the step of concurrently carrying out a second plurality of sequences after said first plurality of sequences have been carried out (FIG. 3) referenced by the second column of Processing Elements 400 which are processed concurrently after the completion of the first column of Processing Elements.

Claim 36, Kerr teaches wherein said first plurality of sequences starts being carried out at a first time (FIG. 5) referenced by the Row 0 IHB to PE_0 starting at time t_1, and said second plurality of sequences starts being carried out at a second time later than said first time (FIG. 5, FIG. 6, column 11 lines 3-22) referenced by the shaded area after Row 5 which is the time for the second column PE processing corresponding to time t_9, by a predetermined period of time (column 11 lines 40-45) referenced by the completion of the first column PE processing with guard time of t_1-t_0.

Claim 43, Kerr teaches a recording medium readable by a computer storing a program therein (FIG. 4) referenced by the Instruction Memory 420 readable by the Memory Manager computer in communication with the CPU Core 410, for causing a computer to act as an arbiter circuit constituting a packet exchanger (FIG. 2, column 6 lines 22-37, column 7 lines 31-42) referenced by the arbiter 255 of the network switch which is a packet exchanger, together with an input buffer temporarily storing a packet having arrived at an input port (FIG. 2, FIG. 3, column 8 lines 36-60) referenced by the Input Header Buffer 700 receiving input data via the Buffer and Queuing Unit 210 from the

input ports, and a packet switch which switches a packet between a specific input port and a specific output port (FIG. 1, FIG. 2, column 5 lines 42-44) referenced by the router/switch 200, said arbiter circuit having functions of (a) concurrently carrying out a first plurality of sequences in each of said sequences basic processes (FIG. 3, column 5 lines 45-49, column 8 lines 36-54, column 9 lines 53-56) referenced by the column of Processing Elements 400 operating in parallel of substantially the same function, for at least one of said input buffer (FIG. 3) referenced by the Input Header Buffer 700, and said output port, (FIG. 3) referenced by the Output Header Buffer 900, are carried out in a predetermined order (FIG. 3) referenced by the fixed row of PE 400 which determines the fixed order of processing, and (b) making an allowance in each of said sequences for packets to be output through output ports at different times from one another (FIG. 6, column 11 lines 3-22) referenced by the phase difference between rows for different output times to the Output Header Buffer 900.

Claim 46, Kerr teaches an arbiter circuit wherein said basic process is completed in a unit period of time defined as a period of time necessary for said input buffers to output a packet (FIG. 3, FIG. 6, column 11 lines 3-22) referenced by the time period of 6 columns for processing to the Output Header Buffer 900 to output from the switch, said basic process being carried out for at least one of said input buffers and said output ports in each of said sequences in said unit period of time (FIG. 3) referenced by the row for the Input Header Buffers 700 to the Output Header Buffers for the unit of time of 6 processing elements.

Claim 47, Kerr teaches an arbiter circuit wherein the arbiter circuit includes a function of concurrently carrying out a second plurality of sequences after said first plurality of sequences have been carried out (FIG. 3) referenced by the second column of Processing Elements 400 which are processed concurrently after the completion of the first column of Processing Elements.

Claim 49, Kerr teaches an arbiter circuit wherein said arbiter circuit starts carrying out said first plurality of sequences at a first time (FIG. 5) referenced by the Row 0 IHB to PE_0 starting at time t_1, and said second plurality of sequences at a second time later than said first time (FIG. 5, FIG. 6, column 11 lines 3-22) referenced by the shaded area after Row 5 which is the time for the second column PE processing corresponding to time t_9, by a predetermined period of time (column 11 lines 40-45) referenced by the completion of the first column PE processing with guard time of t_1-t_0.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 8, 10, 12, 13, 15, 16, 21, 23, 25, 26, 29, 31, 32, 37, 39, 41, 42, 44, 45, 50, 52, 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kerr as applied to claims 1, 4, 5, 7, 14, 17, 18, 20, 30, 33, 34, 36, 43, 46, 47, 49 above, in view of Chao et al. (Patent number 6667984).

Claim 2, Kerr teaches a switch processing engine of basic functions. Kerr does not teach said basic processes includes selecting an output port through which a packet is output from an input port.

Chao teaches a basic process includes the step of (c) selecting an output port through which a packet is output from an input port among output ports not yet occupied by any input buffers (FIGURE 10, column 16 lines 10-24) referenced by Step 1010 selecting a cell from among the head of line cells of the virtual output queues of non-empty virtual queues, said step being to be carried out in input sequential arbitration in which said basic processes are carried out for said input buffers in a predetermined order (FIGURE 10, FIGURE 11, column 16 lines 41-45) referenced by the Dual Round Robin Arbitration Method 1000 wherein each input buffer has arbitration carried out in order.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 3, Kerr teaches a switch processing engine of basic functions. Kerr does not teach said basic processes select an input buffer to be allowed to output a packet through an output port.

Chao teaches a basic process includes the step of selecting an input buffer to be allowed to output a packet through an output port among input buffers not yet allowed to do so (column 15 lines 23-38, FIGURE 10, column 16 lines 10-33, FIGURE 13, column 19 lines 11-19) referenced by Step 1030 wherein the output port choose a winner among the input ports using the optimized input arbitration process 1270' with token tunneling, said step being to be carried out in output sequential arbitration in which said basic processes are carried out for said output ports in a predetermined order (FIGURE 10) referenced by Step 1040 for each output port sending a winning grant to the input port with the output port arbitrated in sequential order.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 8, Kerr teaches a switch processing engine of basic functions. Kerr does not teach selecting an input buffer to be allowed to output a packet having a higher priority.

Chao teaches a basic process includes the steps of (a) selecting an input buffer to be allowed to output a packet having a higher priority among packets accumulated in said input buffers (FIGURE 33, column 31 lines 66-67, column 32 lines 1-12) referenced by

arbiter Step 3310 wherein each column the value of the highest priority is determined, and (b) selecting an input buffer to be allowed to output a packet having a lower priority among packets accumulated in said input buffers (FIGURE 33, column 31 lines 42-63) referenced by Step 3330 wherein token ring round robin is used and the cells in the column at the determined highest level priority will contend for the output port which implies priority levels of less than the maximum.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 10, Kerr teaches a switch processing engine of basic functions. Kerr does not teach selecting an input buffer to be allowed to output a packet having a higher priority. Chao teaches (c1) carrying out said basic processes for all of said input buffers with respect to a packet having a higher priority (FIGURE 9, column 15 lines 46-61, FIGURE 33, column 31 lines 66-67, column 32 lines 1-12) referenced by arbiter Step 3310 wherein each column the value of the highest priority is determined for processing through the switch matrix, and (c2) carrying out said basic processes for all of said input buffers with respect to a packet having a lower priority (FIGURE 33, column 31 lines 42-63) referenced by Step 3330 wherein token ring round robin is used and the cells in the column at the determined highest level priority will contend for the output port which implies priority levels of less than the maximum being a lower priority.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 12, Kerr teaches each of said basic processes is completed in a unit of period of time defined as a period of time necessary for said input buffers to output a packet (FIG. 3, FIG. 6, column 11 lines 3-22) referenced by the time period of 6 columns for processing to the Output Header Buffer 900 to output from the switch. Kerr does not teach another sequence starts being carried out after said step (c1) have been completed.

Chao teaches another sequence starts being carried out after said step (c1) have been completed (FIGURE 33) referenced by the multiple priority level arbitration method 3300 which is repeated for each packet cell determination of the output port.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 13, Kerr teaches a switch processing engine of basic functions. Kerr does not teach the number of sequences is equal to the number of ports.

Chao teaches the number of sequences is equal to the number of ports in said packet exchanger (FIGURE 9, column 15 lines 45-61, FIGURE 10) referenced by the number of N input ports 910 and the number N output ports wherein the number of virtual output queues 912 is based on the number of output ports 930 and wherein the arbitration is performed round robin for each input port.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 15, Kerr teaches a switch processing engine of basic functions. Kerr does not teach selection of an output port through which a packet is output from an input port. Chao teaches an arbiter circuit (Title) referenced by the apparatus for arbitrating an output port, wherein an output port through which a packet is output from an input port is selected among output ports not yet occupied by any input buffers (FIGURE 10, column 16 lines 10-24) referenced by Step 1010 selecting a cell from among the head of line cells of the virtual output queues of non-empty virtual queues, in each of said basic processes which are carried out for said input buffers in a predetermined order (FIGURE 10, FIGURE 11, column 16 lines 41-45) referenced by the Dual Round Robin Arbitration Method 1000 wherein each input buffer has arbitration carried out in order.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch

processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 16, Kerr teaches a switch processing engine of basic functions. Kerr does not teach an arbiter selects an input buffer to be allowed to output a packet through an output port.

Chao teaches an arbiter circuit includes the step of selecting an input buffer to be allowed to output a packet through an output port among input buffers not yet allowed to do so (column 15 lines 23-38, FIGURE 10, column 16 lines 10-33, FIGURE 13, column 19 lines 11-19) referenced by Step 1030 wherein the output port choose a winner among the input ports using the optimized input arbitration process 1270' with token tunneling, in each of said basic processes which are carried out for said output ports in a predetermined order (FIGURE 10) referenced by Step 1040 for each output port sending a winning grant to the input port with the output port arbitrated in sequential order.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 21, Kerr teaches a switch processing engine of basic functions. Kerr does not teach selecting an input buffer to be allowed to output a packet having a higher priority.

Chao teaches an arbiter wherein said arbiter circuit selects an input buffer to be allowed to output a packet having a higher priority among packets accumulated in said input buffers (FIGURE 33, column 31 lines 66-67, column 32 lines 1-12) referenced by arbiter Step 3310 wherein each column the value of the highest priority is determined, and then selects an input buffer to be allowed to output a packet having a lower priority among packets accumulated in said input buffers in each o f said basic processes (FIGURE 33, column 31 lines 42-63) referenced by Step 3330 wherein token ring round robin is used and the cells in the column at the determined highest level priority will contend for the output port which implies priority levels of less than the maximum with arbitration method 3300 forming a basic process.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 23, Kerr teaches a switch processing engine of basic functions. Kerr does not teach selecting an input buffer to be allowed to output a packet having a higher priority. Chao teaches an arbiter circuit wherein said arbiter circuit carries out said basic processes for all of said input buffers firstly with respect to a packet having a higher priority (FIGURE 9, column 15 lines 46-61, FIGURE 33, column 31 lines 66-67, column 32 lines 1-12) referenced by arbiter Step 3310 wherein each column the value of the highest priority is determined for processing through the switch matrix, and secondly

with respect to a packet having a lower priority (FIGURE 33, column 31 lines 42-63) referenced by Step 3330 wherein token ring round robin is used and the cells in the column at the determined highest level priority will contend for the output port which implies priority levels of less than the maximum being a lower priority.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 25, Kerr teaches an arbiter circuit carrying out each of said basic processes in a unit of period of time defined as a period of time necessary for said input buffers to output a packet (FIG. 3, FIG. 6, column 11 lines 3-22) referenced by the time period of 6 columns for processing to the Output Header Buffer 900 to output from the switch, and starts carrying out another sequence after said basic processes have been completed (FIG. 2, FIG. 3) referenced by the processing of another packet from the Buffer and Queuing Unit 210 by the Arrayed Processing Engine 300.

Claim 26, Kerr teaches a switch processing engine of basic functions. Kerr does not teach a plurality of unit modules connecting to one another in a ring.
Chao teaches an arbiter circuit includes (a) a plurality of unit modules each associated with at least one of said input buffer and said output port each of said unit modules carrying out said basic processes (FIGURE 9) referenced by the input port controllers

with input queues 910 each with a separate queue 912 associated to an output port 930, and (b) a signal line connecting said unit modules to one another in a ring (Figure 22A) referenced by the modules passing a token in a round robin mode wherein the modules are in a ring structure and the line signal is representative of the token.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 29, Kerr teaches an arbiter in a switch processing engine of basic functions. Kerr does not teach the number of sequences is equal to the number of ports.
Chao teaches the number of sequences is equal to the number of ports in said packet exchanger (FIGURE 9, column 15 lines 45-61, FIGURE 10) referenced by the number of N input ports 910 and the number N output ports wherein the number of virtual output queues 912 is based on the number of output ports 930 and wherein the arbitration is performed round robin for each input port.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 31, Kerr teaches a switch processing engine of basic functions. Kerr does not teach said basic processes includes selecting an output port through which a packet is output from an input port.

Chao teaches a basic process includes the step of (c) selecting an output port through which a packet is output from an input port among output ports not yet occupied by any input buffers (FIGURE 10, column 16 lines 10-24) referenced by Step 1010 selecting a cell from among the head of line cells of the virtual output queues of non-empty virtual queues, said step being to be carried out in input sequential arbitration in which said basic processes are carried out for said input buffers in a predetermined order (FIGURE 10, FIGURE 11, column 16 lines 41-45) referenced by the Dual Round Robin Arbitration Method 1000 wherein each input buffer has arbitration carried out in order.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 32, Kerr teaches a switch processing engine of basic functions. Kerr does not teach said basic processes select an input buffer to be allowed to output a packet through an output port.

Chao teaches a basic process includes the step of selecting an input buffer to be allowed to output a packet through an output port among input buffers not yet allowed to do so (column 15 lines 23-38, FIGURE 10, column 16 lines 10-33, FIGURE 13, column

19 lines 11-19) referenced by Step 1030 wherein the output port choose a winner among the input ports using the optimized input arbitration process 1270' with token tunneling, said step being to be carried out in output sequential arbitration in which said basic processes are carried out for said output ports in a predetermined order (FIGURE 10) referenced by Step 1040 for each output port sending a winning grant to the input port with the output port arbitrated in sequential order.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 37, Kerr teaches a switch processing engine of basic functions. Kerr does not teach selecting an input buffer to be allowed to output a packet having a higher priority. Chao teaches a basic process includes the steps of (a) selecting an input buffer to be allowed to output a packet having a higher priority among packets accumulated in said input buffers (FIGURE 33, column 31 lines 66-67, column 32 lines 1-12) referenced by arbiter Step 3310 wherein each column the value of the highest priority is determined, and (b) selecting an input buffer to be allowed to output a packet having a lower priority among packets accumulated in said input buffers (FIGURE 33, column 31 lines 42-63) referenced by Step 3330 wherein token ring round robin is used and the cells in the column at the determined highest level priority will contend for the output port which implies priority levels of less than the maximum.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 39, Kerr teaches a switch processing engine of basic functions. Kerr does not teach selecting an input buffer to be allowed to output a packet having a higher priority. Chao teaches (c1) carrying out said basic processes for all of said input buffers with respect to a packet having a higher priority (FIGURE 9, column 15 lines 46-61, FIGURE 33, column 31 lines 66-67, column 32 lines 1-12) referenced by arbiter Step 3310 wherein each column the value of the highest priority is determined for processing through the switch matrix, and (c2) carrying out said basic processes for all of said input buffers with respect to a packet having a lower priority (FIGURE 33, column 31 lines 42-63) referenced by Step 3330 wherein token ring round robin is used and the cells in the column at the determined highest level priority will contend for the output port which implies priority levels of less than the maximum being a lower priority.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 41, Kerr teaches each of said basic processes is completed in a unit of period of time defined as a period of time necessary for said input buffers to output a packet (FIG. 3, FIG. 6, column 11 lines 3-22) referenced by the time period of 6 columns for processing to the Output Header Buffer 900 to output from the switch. Kerr does not teach another sequence starts being carried out after said step (c1) have been completed.

Chao teaches another sequence starts being carried out after said step (c1) have been completed (FIGURE 33) referenced by the multiple priority level arbitration method 3300 which is repeated for each packet cell determination of the output port.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 42, Kerr teaches a switch processing engine of basic functions. Kerr does not teach the number of sequences is equal to the number of ports.

Chao teaches the number of sequences is equal to the number of ports in said packet exchanger (FIGURE 9, column 15 lines 45-61, FIGURE 10) referenced by the number of N input ports 910 and the number N output ports wherein the number of virtual output queues 912 is based on the number of output ports 930 and wherein the arbitration is performed round robin for each input port.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 44, Kerr teaches a recording medium using a CPU for an arbiter circuit of a switch processing engine of basic functions. Kerr does not teach selection of an output port through which a packet is output from an input port.
Chao teaches an arbiter circuit (Title) referenced by the apparatus for arbitrating an output port, wherein an output port through which a packet is output from an input port is selected among output ports not yet occupied by any input buffers (FIGURE 10, column 16 lines 10-24) referenced by Step 1010 selecting a cell from among the head of line cells of the virtual output queues of non-empty virtual queues, in each of said basic processes which are carried out for said input buffers in a predetermined order (FIGURE 10, FIGURE 11, column 16 lines 41-45) referenced by the Dual Round Robin Arbitration Method 1000 wherein each input buffer has arbitration carried out in order.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 45, Kerr teaches a recording medium using a CPU for an arbiter circuit of a switch processing engine of basic functions. Kerr does not teach an arbiter selects an input buffer to be allowed to output a packet through an output port.
Chao teaches an arbiter circuit wherein an input buffer be allowed to output a packet through an output port is selected among input buffers not yet allowed to do so (column 15 lines 23-38, FIGURE 10, column 16 lines 10-33, FIGURE 13, column 19 lines 11-19) referenced by Step 1030 wherein the output port choose a winner among the input ports using the optimized input arbitration process 1270' with token tunneling, in each of said basic processes which are carried out for said output ports in a predetermined order (FIGURE 10) referenced by Step 1040 for each output port sending a winning grant to the input port with the output port arbitrated in sequential order.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 50, Kerr teaches a recording medium using a CPU for an arbiter circuit of a switch processing engine of basic functions. Kerr does not teach selecting an input buffer to be allowed to output a packet having a higher priority.
Chao teaches an arbiter wherein said arbiter circuit selects an input buffer to be allowed to output a packet having a higher priority among packets accumulated in said input buffers (FIGURE 33, column 31 lines 66-67, column 32 lines 1-12) referenced by arbiter

Step 3310 wherein each column the value of the highest priority is determined, and then selects an input buffer to be allowed to output a packet having a lower priority among packets accumulated in said input buffers in each o f said basic processes (FIGURE 33, column 31 lines 42-63) referenced by Step 3330 wherein token ring round robin is used and the cells in the column at the determined highest level priority will contend for the output port which implies priority levels of less than the maximum with arbitration method 3300 forming a basic process.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 52, Kerr teaches a recording medium using a CPU for an arbiter circuit of a switch processing engine of basic functions. Kerr does not teach selecting an input buffer to be allowed to output a packet having a higher priority.

Chao teaches an arbiter circuit wherein said arbiter circuit carries out said basic processes for all of said input buffers firstly with respect to a packet having a higher priority (FIGURE 9, column 15 lines 46-61, FIGURE 33, column 31 lines 66-67, column 32 lines 1-12) referenced by arbiter Step 3310 wherein each column the value of the highest priority is determined for processing through the switch matrix, and secondly with respect to a packet having a lower priority (FIGURE 33, column 31 lines 42-63) referenced by Step 3330 wherein token ring round robin is used and the cells in the

column at the determined highest level priority will contend for the output port which implies priority levels of less than the maximum being a lower priority.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbitration process method of Chao to the switch processing engine of Kerr for the purpose of arbitrating contention for an output port of a switch.

Claim 54, Kerr teaches a recording medium using a CPU for an arbiter circuit of a switch processing engine of basic functions. Kerr teaches an arbiter circuit carrying out each of said basic processes in a unit of period of time defined as a period of time necessary for said input buffers to output a packet (FIG. 3, FIG. 6, column 11 lines 3-22) referenced by the time period of 6 columns for processing to the Output Header Buffer 900 to output from the switch, and starts carrying out another sequence after said basic processes have been completed (FIG. 2, FIG. 3) referenced by the processing of another packet from the Buffer and Queuing Unit 210 by the Arrayed Processing Engine 300.

Allowable Subject Matter

4. Claims 6, 9, 11, 19, 22, 24, 27, 28, 35, 38, 40, 48, 51, 53, 55-58 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in

independent form including all of the limitations of the base claim and any intervening claims.

Citation of Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Patent number 6072772, Charny et al. discloses a method for providing bandwidth and delay guarantees in a crossbar switch with speedup. Patent number 5278828, Chao discloses a method and system for managing queued cells. Patent number 6330584, Joffe et al. discloses a system and method for multi-tasking, resource sharing and execution of computer instructions. Patent number 5519698, Lyles et al. discloses modification to a reservation ring mechanism for controlling contention in a broadband ISDN fast packet switch suitable for use in a local area network.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John L Shew whose telephone number is 571-272-3137. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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